AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

Listing of Claims:

Claim 1 (Currently Amended): Stereo demultiplexer configured ~~and adapted for receiving~~ to receive a frequency demodulated stereo-multiplex signal ~~($m(t)$)~~ which comprises at least a stereo-difference signal ~~($m_d(t)$)~~, a stereo-sum signal ~~($m_s(t)$)~~ and a pilot carrier, said stereo demulitplexer comprising:

a decimation filter configured to extract, from said frequency demodulated stereo-multiplex signal, a sampling rate decimated signal decimated by a factor D regarding said frequency demodulated stereo-multiplex signal, thereby providing the stereo-sum signal and the pilot carrier signal and eliminating the stereo-difference signal; and

a PLL-circuit configured ~~and adapted~~ to receive said extracted signal as an input signal and for recovering, from said input signal, the pilot carrier or at least one harmonic ~~thereof~~ of the pilot carrier to perform an amplitude demodulation~~, wherein said PLL-circuit receives an input signal that, in essence, solely comprises said stereo-sum signal ($m_s(t)$) and said pilot carrier, wherein said input signal is sampling rate decimated by a decimation factor of D with regard to said received frequency demodulated stereo-multiplex signal~~.

Claim 2 (Currently Amended): Stereo demultiplexer according to claim 1, ~~wherein said sampling rate decimated stereo-sum signal ($m_s(t)$) is further sampling rate decimated by a decimation factor of E before said PLL-circuit receives it as input signal~~ further comprising:

sampling rate decimation means configured to further decimate the sampling rate of said extracted signal by a decimation factor E, before said PLL-circuit receives the signal that passed through the decimation filter and the sampling rate decimation means.

Claim 3 (Currently Amended): Stereo demultiplexer according to claim 1 ~~configured and adapted for receiving a frequency-demodulated stereo-multiplex signal (m(t)) which comprises at least a stereo-difference signal ($m_d(t)$), a stereo-sum signal ($m_s(t)$) and a pilot carrier, comprising a PLL-circuit configured and adapted for recovering the pilot carrier or at least one harmonic thereof to perform an amplitude demodulation, wherein said PLL-circuit receives an input signal that, in essence, solely comprises said stereo-sum signal ($m_s(t)$) and said pilot carrier, wherein said input signal is sampling rate decimated by a decimation factor of D with regard to said received frequency demodulated stereo-multiplex signal,~~

wherein said PLL-circuit ~~outputs~~ is configured to output a recovered pilot carrier which is interpolated so that ~~it~~ the recovered pilot carrier has a sampling rate equal to that of the frequency demodulated stereo-multiplex signal.

Claim 4 (Currently Amended): Stereo demultiplexer according to claim 3, wherein ~~that~~ said PLL-circuit comprises:

means configured to alternately output D-1 or (E·D)-1 interpolated pilot carrier values (y(k/D+1), ..., y(k/D+(D-1))) and one calculated pilot carrier value (y(k/D)) ~~are alternately output~~.

Claim 5 (Currently Amended): Stereo demultiplexer according to claim 4, wherein said PLL-circuit is further configured to perform said interpolation ~~within the PLL-circuit is performed~~ on a basis of a prediction starting at said calculated pilot carrier value.

Claim 6 (Currently Amended): Stereo demultiplexer according to claim 5, further including:

[[-]] a PLL within the PLL-circuit configured to output ~~which outputs~~ a phase signal, and

[[-]] a first sine calculation unit configured to output ~~which outputs~~ said one calculated pilot carrier value (y(k/D)) on ~~the~~ a basis of said phase signal.

Claim 7 (Currently Amended): Stereo demultiplexer according to claim 6, further including:

[[-]] second to D^{th} or $(E \cdot D)^{th}$ sine calculation units each configured to output ~~of which outputs~~ one of said D-1 or (E·D)-1 interpolated pilot carrier values (y(k/D+1), ..., y(k/D+(D-1))) on a basis of said phase signal and a respective added phase shift value.

Claim 8 (Currently Amended): Stereo demultiplexer according to claim 6, further including:

[[-]] a third multiplexer configured to multiplex ~~which multiplies~~ said phase signal with a factor ~~of~~ 2 before the phase signal ~~it~~ is input to said first sine calculation unit or a respective second to D^{th} or $(E \cdot D)^{th}$ sine calculation unit via a respective second to D^{th} or $(E \cdot D)^{th}$ adder, configured to add ~~which adds~~ said respective phase shift value so that the 2^{nd} harmonic of the pilot carrier is generated.

Claim 9 (Currently Amended): Stereo demultiplexer according to claim 6, wherein said PLL comprises:

[[-]] a first multiplier configured to receive ~~receiving~~ samples of the stereo-sum signal ~~(x(k))~~ as multiplicant at a first input,

[[-]] a filter ~~receiving~~ configured to receive the output signal of said first multiplier,

[[-]] a second multiplier ~~multiplying~~ configured to multiply said output signal of said filter with a PLL gain ~~(PLL_loop_gain)~~,

[[-]] a first adder ~~receiving~~ configured to receive said output signal of said second multiplier at a first input as a first summand, configured to receive a constant representing the product of ~~the~~ a pilot carrier frequency ~~(ω_{pil})~~ and the sampling period at a second input as a second summand, and configured to receive a delayed phase signal which is the output signal of said first adder at a third input as a third summand,

[[-]] a delay element ~~receiving~~ configured to receive said phase signal of said first adder and configured to supply ~~supplying~~ said delayed phase signal to said third input of said first adder, and

[[-]] a cosine calculation unit ~~receiving~~ configured to receive the phase signal of said first adder and configured to supply ~~supplying its~~ an output signal of the cosine calculation unit as multiplier to a second input of said first multiplier.

Claims 10-19 (Canceled).

Claim 20 (Currently Amended): Stereo demultiplexer according to claim 6, including

[[-]] a third multiplexer configured to multiply ~~which multiplies~~ said phase signal with a factor ~~of~~ 2 before the phase signal ~~it~~ is input to said first sine calculation unit and a respective second to D^{th} or $(E \cdot D)^{th}$ sine calculation unit via a respective second to D^{th} or $(E \cdot D)^{th}$ adder ~~which adds~~ configured to add said respective phase shift value so that the 2^{nd} harmonic of the pilot carrier is generated.

Claim 21 (Currently Amended): The stereo demultiplexer of claim 1, further comprising:

channel recovery means configured to recover ~~and adapted for recovering~~ a left or right channel associated with said stereo-multiplex signal on a ~~the~~ basis of first and second intermediate signals; and

a sampling rate decimator configured to decimate a ~~and adapted for~~ sampling rate ~~decimating~~ of one of said first and second intermediate signals by a decimation factor E_x and ~~supplying~~ configured to supply said sampling rate decimated intermediate signal to said PLL-circuit as said input signal.

Claim 22 (Currently Amended): The stereo demultiplexer of claim 21, wherein said channel recovery means is an adder configured to receive ~~and adapted for receiving~~ said first and second intermediate signals as an input.

Claim 23 (Currently Amended): The stereo demultiplexer of claim 1, further comprising:

channel recovery means configured to recover ~~and adapted for recovering~~ a left or right channel associated with said stereo-multiplex signal on the basis of first and second intermediate signals,

wherein said input signal is one of said first and second intermediate signals.

Claim 24 (Currently Amended): The stereo demultiplexer of claim 23, wherein said channel recovery means is an adder configured to receive ~~and adapted for receiving~~ said first and second intermediate signals as an input.

Claim 25 (Currently Amended): The stereo demultiplexer of claim 1, wherein said PLL-circuit is configured to output ~~outputs~~ a recovered pilot carrier which is interpolated so

that ~~it~~ the recovered pilot carrier has a sampling rate equal to that of the frequency demodulated stereo-multiplex signal.